What is claimed is:

1. A semiconductor wafer structure, comprising:

at least one bipolar transistor defined in said semiconductor wafer structure;

at least one CMOS transistor device defined in said semiconductor wafer structure;

said CMOS transistor device being comprised of a thin film of semiconductor on an insulating layer;

each transistor of said CMOS transistor device being defined in said thin film and including spaced apart source and drain regions and an intermediate channel region, each said region being the thickness of said thin film; and

a respective gate disposed on an oxide film on said channel region of each said CMOS transistor device; and

a plurality of electrodes connected to selected elements of said bipolar transistor and said CMOS transistor device.

2. A wafer structure according to claim 1 wherein:

said bipolar transistor includes a base;

said base being of a silicon- germanium semiconductor material.

3. A wafer structure according to claim 1 wherein:

the thickness of said thin film of semiconductor is no more than 3000 Å.

4. A wafer structure according to claim 3 wherein:

the thickness of said thin film of semiconductor is around 1000 Å.

5. A wafer structure according to claim 1 wherein:

said CMOS transistor device includes first and second MOS transistors each having a source and drain region of a different conductivity type than its channel region.

6. A wafer structure according to claim 1 wherein:

said insulating layer is on a substrate;

said substrate has a relatively high resistivity of around 1500 ohm-cm, or greater.

7. A method of fabricating a semiconductor wafer structure having at least one bipolar transistor, which includes a collector, base and emitter, and at least one CMOS transistor device defined in the same wafer structure, comprising the steps of:

fabricating said CMOS transistor device with source, drain and channel regions of each transistor of said CMOS transistor device being contained within a thin film of semiconductor material;

fabricating said bipolar transistor with a plurality of semiconductor layers of predetermined conductivities, without any of said semiconductor layers of said bipolar transistor, during fabrication, extending into the area occupied by said CMOS transistor device.

8. A method according to claim 7, which includes the steps of:

providing a semiconductor structure having a substrate with a semiconductor on insulator layer arrangement on a surface thereof;

depositing a protective oxide layer over said semiconductor on insulator layer arrangement;

removing a portion of said deposited oxide layer, semiconductor and insulator to form a well down to said surface of said substrate, in the area where said bipolar transistor is to be fabricated;

forming a low resistivity layer in said substrate at the bottom of said well;

selectively forming an epitaxial layer in said well on said low resistivity layer and confined to said bipolar transistor area;

forming a collector within said epitaxial layer;

removing said deposited oxide layer;

selectively removing said semiconductor on said insulator in a pattern so as to define two individual islands of semiconductor;

fabricating said CMOS transistor device utilizing said islands of semiconductor;

fabricating said base and emitter of said bipolar transistor;

establishing electrical contact with elements of said bipolar transistor and said CMOS transistor device.

9. A method according to claim 8, which includes the step of:

selectively forming said epitaxial layer only in said well to the exclusion of other areas of said structure.

10. A method according to claim 8, which includes the steps of:

forming said epitaxial layer over said low resistivity layer and said deposited oxide layer; and

thereafter removing said epitaxial layer formed over said deposited oxide layer.

11. A method according to claim 8, which includes the step of:

providing a semiconductor structure having a substrate with a semiconductor on insulator layer arrangement on a surface thereof, where the the thickness of said semiconductor on said insulator is no more than 3000 Å.

12. A method according to claim 11, which includes the step of:

providing a semiconductor structure having a substrate with a semiconductor on insulator layer arrangement on a surface thereof, where the the thickness of said semiconductor on said insulator is no more than around 1000 Å.